CLAIMS

What is claimed is:

1. A digital baseband (DBB) receiver for receiving and processing a wireless communication signal, the DBB receiver comprising:

(a) a demodulator which outputs analog real and imaginary signal components in response to receiving the communication signal;

(b) a first analog low pass filter (LPF) which receives the analog real signal component from the demodulator and outputs a distorted analog real signal component;

(c) a second analog LPF which receives the analog imaginary signal component from the demodulator and outputs a distorted analog imaginary signal component;

(d) a first digital gain control circuit which receives the distorted analog real signal component from the first analog LPF and outputs a processed distorted digital real signal component;

(e) a second digital gain control circuit which receives the distorted analog imaginary signal component from the second analog LPF and outputs a processed distorted digital imaginary signal component; and

(f) a digital time domain compensation module which receives the processed distorted digital real and imaginary signal components and outputs digital real and imaginary compensated signal components, wherein the digital time domain compensation module removes group delay variation distortion, introduced by the first and second analog LPFs, from the real and imaginary signal components.

2. The DBB receiver of claim 1 wherein the digital time domain compensation module comprises:

(i) a real signal path;

(ii) a plurality of real signal component delay units connected in series along the real signal path;

(iii) a plurality of real filter coefficient positions;

(iv) a first combiner having a plurality of inputs; and

(v) a plurality of active real filter coefficient units located at a subset of the real filter coefficient positions, wherein each of the active real filter coefficient units has an input connected to the real signal path and an output connected to one of the inputs of the first combiner, and the first combiner outputs the real compensated signal component.

3. The DBB receiver of claim 2 wherein the digital time domain compensation module further comprises:

(vi) an imaginary signal path;

(vii) a plurality of imaginary signal component delay units connected in series along the imaginary signal path;

(viii) a plurality of imaginary filter coefficient positions;

(ix) a second combiner having a plurality of inputs; and

(x) a plurality of active imaginary filter coefficient units located at a subset of the imaginary filter coefficient positions, wherein each of the active imaginary filter coefficient units has an input connected to the imaginary signal path and an output connected to one of the inputs of the second combiner, and the second combiner outputs the imaginary compensated signal component.

4. The DBB receiver of claim 1 wherein the digital time domain compensation module includes a plurality of real filter coefficient unit positions and a plurality of imaginary filter coefficient unit positions, wherein a plurality of active real filter coefficient units are present at a subset of the real filter coefficient unit positions and a plurality of active imaginary filter coefficient units are present at a subset of the imaginary filter coefficient unit positions.

5. The DBB receiver of claim 4 wherein the digital time domain compensation module further includes a plurality of real signal component delay units and a plurality of imaginary signal component delay units having inputs and outputs connected to the inputs of respective ones of the active filter coefficient units.

6. The DBB receiver of claim 1 wherein the digital time domain compensation module is a finite impulse response (FIR) filter having characteristics which are selected such that the frequency domain response of the digital time domain compensation module is the inverse of the frequency domain response of the analog LPFs.

7. The DBB receiver of claim 1 wherein the first digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog real signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog real signal component to a compressed distorted digital real signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital real signal component.

8. The DBB receiver of claim 1 wherein the second digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog imaginary signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog imaginary signal component to a compressed distorted digital imaginary signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital imaginary signal component.

9. A wireless transmit/receive unit (WTRU) for receiving and processing a wireless communication signal, the WTRU comprising:

(a) a demodulator which outputs analog real and imaginary signal components in response to receiving the communication signal;

(b) a first analog low pass filter (LPF) which receives the analog real signal component from the demodulator and outputs a distorted analog real signal component;

(c) a second analog LPF which receives the analog imaginary signal component from the demodulator and outputs a distorted analog imaginary signal component;

(d) a first digital gain control circuit which receives the distorted analog real signal component from the first analog LPF and outputs a processed distorted digital real signal component;

(e) a second digital gain control circuit which receives the distorted analog imaginary signal component from the second analog LPF and outputs a processed distorted digital imaginary signal component; and

(f) a digital time domain compensation module which receives the processed distorted digital real and imaginary signal components and outputs digital real and imaginary compensated signal components, wherein the digital time domain compensation module removes group delay variation distortion, introduced by the first and second analog LPFs, from the real and imaginary signal components.

10. The WTRU of claim 9 wherein the digital time domain compensation module comprises:

(i) a real signal path;

(ii) a plurality of real signal component delay units connected in series along the real signal path;

(iii) a plurality of real filter coefficient positions;

(iv) a first combiner having a plurality of inputs; and

(v) a plurality of active real filter coefficient units located at a subset of the real filter coefficient positions, wherein each of the active real filter coefficient units has an input connected to the real signal path and an output connected to one of the inputs of the first combiner, and the first combiner outputs the real compensated signal component.

11. The WTRU of claim 10 wherein the digital time domain compensation module further comprises:

(vi) an imaginary signal path;

(vii) a plurality of imaginary signal component delay units connected in series along the imaginary signal path;

(viii) a plurality of imaginary filter coefficient positions;

(ix) a second combiner having a plurality of inputs; and

(x) a plurality of active imaginary filter coefficient units located at a subset of the imaginary filter coefficient positions, wherein each of the active imaginary filter coefficient units has an input connected to the imaginary signal path and an output connected to one of the inputs of the second combiner, and the second combiner outputs the imaginary compensated signal component.

12. The WTRU of claim 9 wherein the digital time domain compensation module includes a plurality of real filter coefficient unit positions and a plurality of imaginary filter coefficient unit positions, wherein a plurality of active real filter coefficient units are present at a subset of the real filter coefficient unit positions and a plurality of active imaginary filter coefficient units are present at a subset of the imaginary filter coefficient unit positions.

13. The WTRU of claim 12 wherein the digital time domain compensation module further includes a plurality of real signal component delay units and a plurality of imaginary signal component delay units having inputs and outputs connected to the inputs of respective ones of the active filter coefficient units.

14. The WTRU of claim 9 wherein the digital time domain compensation module is a finite impulse response (FIR) filter having characteristics which are selected such that the frequency domain response of the digital time domain compensation module is the inverse of the frequency domain response of the analog LPFs.

15. The WTRU of claim 9 wherein the first digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog real signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog real signal component to a compressed distorted digital real signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital real signal component.

16. The WTRU of claim 9 wherein the second digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog imaginary signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog imaginary signal component to a compressed distorted digital imaginary signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital imaginary signal component.

17. An integrated circuit (IC) for receiving and processing a wireless communication signal, the IC comprising:

(a) a demodulator which outputs analog real and imaginary signal components in response to receiving the communication signal;

(b) a first analog low pass filter (LPF) which receives the analog real signal component from the demodulator and outputs a distorted analog real signal component;

(c) a second analog LPF which receives the analog imaginary signal component from the demodulator and outputs a distorted analog imaginary signal component;

(d) a first digital gain control circuit which receives the distorted analog real signal component from the first analog LPF and outputs a processed distorted digital real signal component;

(e) a second digital gain control circuit which receives the distorted analog imaginary signal component from the second analog LPF and outputs a processed distorted digital imaginary signal component; and

(f) a digital time domain compensation module which receives the processed distorted digital real and imaginary signal components and outputs digital real and imaginary compensated signal components, wherein the digital time domain compensation module removes group delay variation distortion, introduced by the first and second analog LPFs, from the real and imaginary signal components.

18. The IC of claim 17 wherein the digital time domain compensation module comprises:

(i) a real signal path;

(ii) a plurality of real signal component delay units connected in series along the real signal path;

(iii) a plurality of real filter coefficient positions;

(iv) a first combiner having a plurality of inputs; and

(v) a plurality of active real filter coefficient units located at a subset of the real filter coefficient positions, wherein each of the active real filter coefficient units has an input connected to the real signal path and an output connected to one of the inputs of the first combiner, and the first combiner outputs the real compensated signal component.

19. The IC of claim 18 wherein the digital time domain compensation module further comprises:

(vi) an imaginary signal path;

(vii) a plurality of imaginary signal component delay units connected in series along the imaginary signal path;

(viii) a plurality of imaginary filter coefficient positions;

(ix) a second combiner having a plurality of inputs; and

(x) a plurality of active imaginary filter coefficient units located at a subset of the imaginary filter coefficient positions, wherein each of the active imaginary filter coefficient units has an input connected to the imaginary signal path and an output connected to one of the inputs of the second combiner, and the second combiner outputs the imaginary compensated signal component.

20. The IC of claim 17 wherein the digital time domain compensation module includes a plurality of real filter coefficient unit positions and a plurality of imaginary filter coefficient unit positions, wherein a plurality of active real filter coefficient units are present at a subset of the real filter coefficient unit positions and a plurality of active imaginary filter coefficient units are present at a subset of the imaginary filter coefficient unit positions.

21. The IC of claim 20 wherein the digital time domain compensation module further includes a plurality of real signal component delay units and a plurality of imaginary signal component delay units having inputs and outputs connected to the inputs of respective ones of the active filter coefficient units.

22. The IC of claim 17 wherein the digital time domain compensation module is a finite impulse response (FIR) filter having characteristics which are selected such that the frequency domain response of the digital time domain compensation module is the inverse of the frequency domain response of the analog LPFs.

23. The IC of claim 17 wherein the first digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog real signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog real signal component to a compressed distorted digital real signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital real signal component.

24. The IC of claim 17 wherein the second digital gain control circuit comprises:

(i) a logarithmic amplifier for compressing the distorted analog imaginary signal component from a wider dynamic range to a lower dynamic range;

(ii) an analog to digital converter (ADC) for converting the compressed distorted analog imaginary signal component to a compressed distorted digital imaginary signal component; and

(iii) a look up table (LUT) which provides an anti-log function used to decompress the compressed distorted digital imaginary signal component.